PTO/SB/33 (08-08)

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
15114H-071400US

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on September 22, 2008

Signature /Dana Kane/

Typed or printed name Dana Kane

Application Number	Filed
10/749,910	12/30/2003

First Named Inventor
Kulwinder DHANOA

Art Unit	Examiner
2181	Chun Kuan Lee

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record.
Registration number 57,301.

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34. _____

/Adam Pyonin/
Signature

Adam Pyonin
Typed or printed name

415-576-0200
Telephone number

09/22/2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

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TOWNSEND and TOWNSEND and CREW LLP

By: [signature]

STATEMENT OF REASONS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

PATENT
Attorney Docket No.: 15114H-071400US
Haseltine Lake Ref. No.: A100052GB00/DCO
Altera Ref. No.: A00985

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No. 1395
DHANOA, Kulwinder	Examiner: Chun-Kuan (Mike) Lee
Application No.: 10/749,910	Technology Center/Art Unit: 2181
Filed: December 30, 2003	STATEMENT OF REASONS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW
For: SDRAM Controller	
Customer No.: 26059	

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Final Office Action mailed May 21, 2008 on the above-referenced application, please enter the following:

This statement is submitted in support of the Pre-Appeal Brief Request for Review, which is submitted herewith, along with a Notice of Appeal. The applicant respectfully requests review of the Final Office Action, regarding the rejection of the claims under 35 U.S.C. § 103(a) using *Gray* (U.S. Pat. No. 6,816,923) in view of *Iizuka* (U.S. Pat. No. 5,581,530) and further in view of *Nguyen* (U.S. Pat. No. 5,335,326).

Rejection under 35 U.S.C. § 103

Claims 1, 2, 7-8, 13-14, and 16 are rejected under 35 U.S.C. 103(a) as being obvious over *Gray* (U.S. Pat. No. 6,816,923) in view of *Iizuka* (U.S. Pat. No. 5,581,530) and further in view of *Nguyen* (U.S. Pat. No. 5,335,326). Applicants respectfully submit that these references do not teach or suggest each element of these claims.

Claim 1 recites,

> a plurality of buffers in the memory interface, **each of the plurality of buffers sized to store a data burst for a memory access request, each of the plurality of buffers further including a plurality of sub-buffers** each sized to store a data beat of the data burst stored in the corresponding buffer;
>
> wherein, for **a wrapping memory access request requiring multiple buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer** by the control logic, the **beginning and end data for the memory access request being stored concurrently from a single data burst in the respective sub-buffers of the single respective buffer by the memory interface**, the storing of the beginning and end data in a single buffer avoiding the need for an additional data burst to obtain the end data, the data required for the end of the wrapping memory access request being cached in the respective sub-buffer until needed for transfer in response to the wrapping memory access request

(*emphasis added*).

The Office Action admits that *Gray* does not teach a plurality of buffers sized to store a data burst for a memory access request. The Office Action also admits that *Gray* does not teach that the wrapping memory access request requires multiple buffers and that data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer.

On page 4, the Final Office Action cites *Iizuka* as teaching these features. *Iizuka* discloses a buffer with respect to a hard disk storage device to compensate for slower data transfer between the hard disk and the I/O device. (*Iizuka*, Abstract.) For example, in FIGS 8 and 14, *Iizuka* discloses three **independent** audio tracks of data that interface with a hard disk, and **each track is associated with a respective buffer**. (*Iizuka*, col. 11, lines 21-26.) *Iizuka*

discloses that each buffer is independent of other respective buffers because each track of data is independent from other tracks. (*Iizuka*, col. 10, lines 46-51.)

In other words, track 1 may be **receiving** data from the hard disk while tracks 2 and 3 may be **transmitting** data to the hard disk. (*Iizuka*, col. 14, lines 36-40.) To allow for this independent operation, *Iizuka* teaches that each memory access request between a track and the hard disk is associated with the **individual** track, not a combination of tracks. (*Iizuka*, col. 14, lines 29-40.) Furthermore, because each track of data is independent from the other tracks, each respective buffer of each track is also **independent**. (*Iizuka*, col. 10, lines 46-51.) Thus, ***Iizuka* teaches use of a single buffer associated with each memory access** (or DMA transfer).

Because *Iizuka* discloses a **single** buffer associated with each memory access, the Office Action assertion on page 4 that a DMA transfer is equivalent to a "wrapping memory access request" fails because **claim 1 recites "a wrapping memory access request requiring multiple buffers**." As discussed above, a DMA transfer moves data to/from a **single** buffer. (*Iizuka*, col. 26, lines 4-14.) **Because a DMA transfer discloses a single buffer, a DMA transfer cannot teach a wrapping memory access request requiring multiple buffers**, as recited in claim 1.

Furthermore, *Iizuka* does not teach or suggest "data required for each of a **beginning and an end of the wrapping memory access request** are assigned to respective sub-buffers of a single respective buffer." On page 5, the Office Action asserts that the data block shown in FIG 8 discloses beginning and end data in a single buffer, **but this assertion requires the entire memory access request to be contained in a single buffer**. As discussed above, **claim 1 recites a wrapping memory access request requiring multiple buffers**. Thus, the single buffer shown in FIG 8 does not disclose beginning and end data in a single buffer for a wrapping memory access request that requires multiple buffers.

Even if the buffers associated with the other audio tracks are considered to comprise "multiple buffers" that receive a memory access request, *Iizuka* still does not teach beginning and end data for multiple audio tracks being assigned to a **single** respective buffer. As shown in FIG 14, data is transferred from the first buffer in FIG 14(a). Then, data is transferred from the second buffer in FIG 14(b). Finally, data is transferred from a third buffer in FIG 14(c).

As seen in FIG 14, the beginning data is transferred from a first buffer, and end data is transferred from a third buffer. There is no teaching or suggestion for beginning and end data assigned to a single buffer as recited in claim 1.

Moreover, assuming for the sake of argument that the transfer of data in FIG 14 began and concluded with a first track associated with a single buffer, *Iizuka* does not disclose "the beginning and end data for the memory access request being stored **concurrently from a single data burst** in the respective sub-buffers of the single respective buffer by the memory interface." As shown in FIG 14, *Iizuka* discloses that data is transferred from the buffers in a sequential manner starting with track 1, then track 2, then track 3, and then back to track 1, etc. Because of the sequential nature of the data transfer, *Iizuka* discloses that the beginning data for the first track would be transferred at a first time, and the end data would be transferred at a subsequent time. Therefore, *Iizuka* cannot teach a **concurrent** data transfer of beginning and end data of a memory access request requiring **multiple** buffers.

In addition, *Nguyen* also fails to provide such teaching to make up for the deficiencies in the references with respect to Applicant's claim 1. The Office Action combines *Nguyen* in an attempt to show the use of a pointer as recited in Applicant's claim 1. *Nguyen* teaches a bus-to-bus interface including a central buffer means including first and second FIFO devices, utilizing a pointer means to traverse a circular queue in the FIFO devices slot by slot. (*Nguyen*, col. 1, line 59 - col. 2, line 49.) As previously discussed on page 10 of the Amendment filed on February 11, 2008, *Nguyen*, even given the broadest possible interpretation, cannot show

> wherein, for **a wrapping memory access request requiring multiple buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer** by the control logic, the **beginning and end data for the memory access request being stored concurrently from a single data burst in the respective sub-buffers of the single respective buffer by the memory interface**

(*emphasis added).*

Thus, even if for sake of argument there is motivation to combine *Iizuka* with *Gray* and *Nguyen*, the combination would still fail to teach, suggest, or provide motivation for

each and every element of claim 1. For at least these reasons, claim 1 is allowable. As claim 1 is allowable, dependent claims 2, 5, and 6 are also allowable for at least the same rationale.

Applicant submits that independent claims 7 and 13 should be allowable for at least some of the reasons mentioned above with respect to claim 1. As claim 7 is allowable, dependent claims 8, 11, and 12 are allowable for at least the same rationale.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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